

PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

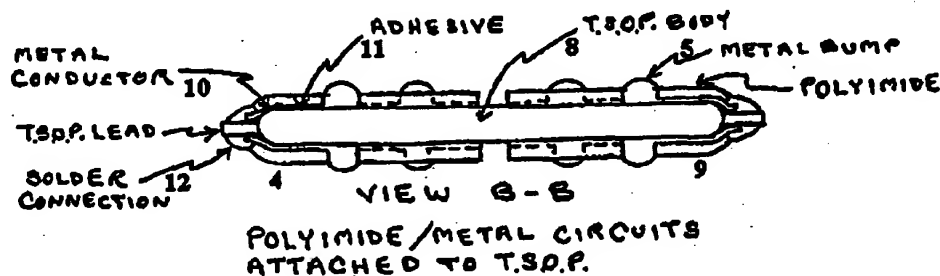


INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : H05K 1/11, H01L 23/12		A1	(11) International Publication Number: WO 99/65282
			(43) International Publication Date: 16 December 1999 (16.12.99)
(21) International Application Number: PCT/US99/13171			(81) Designated States: JP, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).
(22) International Filing Date: 10 June 1999 (10.06.99)			
(30) Priority Data: 09/095,416 10 June 1998 (10.06.98) US			
(71) Applicant: IRVINE SENSORS CORPORATION [US/US]; Building 3, 3001 Redhill Avenue, Costa Mesa, CA 92626-4529 (US).			
(72) Inventor: EIDE, Floyd; 3889 Mistral Drive, Huntington Beach, CA 92649 (US).			
(74) Agent: ANDRAS, Joseph, C.; Myers, Dawes & Andras LLP, Suite 650, 650 Town Center Drive, Costa Mesa, CA 92626 (US).			Published <i>With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>

BEST AVAILABLE COPY

(54) Title: IC STACK UTILIZING FLEXIBLE CIRCUITS WITH BGA CONTACTS



(57) Abstract

A structure and process are disclosed in which IC chip-containing layers are stacked to create electronic density. Each layer is fabricated by forming one or more flexible circuit (4, 9) around a TSOP (8). Each flexible circuit (4, 9) contains conductors (10) which are disposed to connect with TSOP leads, transpose signals to or from various locations on the top or bottom of the TSOP (8), and/or terminate in ball grid contacts (5) for connection to other layers in the stack. The flexible circuits (4, 9) are bonded to the TSOP (8) such that ball grid contacts (5) are exposed on the top and bottom of the TSOP (8), and the ball grid array contacts (5) on the bottom of the lowest layer are disposed to facilitate connection with a PCB or other circuitry.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece			TR	Turkey
BG	Bulgaria	HU	Hungary	ML	Mali	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MN	Mongolia	UA	Ukraine
BR	Brazil	IL	Israel	MR	Mauritania	UG	Uganda
BY	Belarus	IS	Iceland	MW	Malawi	US	United States of America
CA	Canada	IT	Italy	MX	Mexico	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NE	Niger	VN	Viet Nam
CG	Congo	KE	Kenya	NL	Netherlands	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NO	Norway	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	NZ	New Zealand		
CM	Cameroon			PL	Poland		
CN	China	KR	Republic of Korea	PT	Portugal		
CU	Cuba	KZ	Kazakhstan	RO	Romania		
CZ	Czech Republic	LC	Saint Lucia	RU	Russian Federation		
DE	Germany	LI	Liechtenstein	SD	Sudan		
DK	Denmark	LK	Sri Lanka	SE	Sweden		
EE	Estonia	LR	Liberia	SG	Singapore		

1 IC STACK UTILIZING FLEXIBLE CIRCUITS WITH BGA CONTACTS

2
3 Background of the Invention

4 This invention relates to the stacking of layers containing IC
5 (integrated circuit) chips, thereby obtaining high density electronic circuitry. In
6 general, the goal of the present invention is to combine high circuit density with
7 reasonable cost. A unique aspect of this invention is that it stacks IC layers as
8 TSOP's (thin small outline packages) in a footprint smaller than the TSOP
9 footprint itself. Cost reduction is accomplished by relatively low cost forming of
10 individual layers and the ability to incorporate off-the-shelf prepackaged and
11 pre-tested IC's into stacks.

12 Another aspect of successful stacking of chip-containing layers is
13 the ability of the BGA (ball grid array) interconnection to cheaply provide a large
14 number of non-common (non-bussed) connections between individual layers
15 themselves and the substrate to which the stack is attached.

16 The prior art contains several examples where a flexible circuit is
17 used to interconnect unpackaged chips. Yamaji Patent No. 5,394,303 shows a
18 structure in which a flexible film with wiring layers is wrapped around a
19 semiconductor chip, providing an increase in the number of terminals and a
20 second surface for interconnections. McMahon Patent No. 5,362,656 shows a
21 structure in which a flexible circuit is used to route signals from interconnections
22 with the top surface of the chip to ball connectors below the chip substrate.
23 Paurus et al. Patent No. 5,448,511 and Kimura Patent No. 5,313,416 disclose
24 schemes for creating a memory stack by interconnecting a series of memory

1 devices or memory IC chips on a fan-folded flexible circuit board which carries
2 the signals from the various IC chips to each other and out the bottom of the
3 stack to the main PCB. Behelen et al. Patent No. 5,598,033 shows a structure
4 in which a flexible circuit is used to interconnect a semiconductor IC die to BGA
5 contacts on another die displaced laterally, so that two stacks of dice can be
6 interconnected in a zigzag manner.

7 What is not available in the prior art is a stack of IC chip-
8 containing TSOP layers which are fully tested individually prior to stacking, can
9 connect layers in the stack with each other and with the bottom surface of the
10 stack using BGA's, and can provide custom interconnections including the
11 separate connection of individual layer signals to the bottom of the stack. The
12 current invention allows a large I/O count for mixed IC stacking or wide data
13 paths, such as the assembly of wide word memory from layers of memory IC's
14 having smaller word widths. Additionally, the current invention allows stacks
15 having a smaller footprint than their constituent TSOP's, and allows them to be
16 produced at low cost.

17

18 Summary of the Invention

19 This application discloses a version of a fully pre-tested IC-
20 containing layer, which can be stacked and electrically connected by ball grid
21 array contacts on each level of the stack. This application further discloses a
22 method for starting with a standard TSOP package and manufacturing an IC-
23 containing layer with ball grid array contacts ready for stacking with other layers

1 in order to provide a dense electronic package.

2 The TSOP leads are trimmed close to the TSOP body. At this
3 point, the edges of the TSOP body may be mechanically rounded to improve
4 the bending radius of the applied flexible circuit. A flexible circuit containing
5 conductors with exposed sections prepared for joining with the TSOP leads,
6 and other exposed sections prepared with bumps suitable for use as ball grid
7 contacts is fabricated, with the conductors arranged so as to give the desired
8 connections. Using an appropriately shaped heated fixture, the flexible circuit is
9 formed into such a shape that it will slip over one of the lead edges of the
10 TSOP. The flexible circuit is then bonded to the TSOP such that the
11 appropriate exposed conductors of the flexible circuit contact the trimmed leads
12 of the TSOP. The assembly is then dipped into high-melting-temperature solder
13 in order to accomplish a soldered connection between the trimmed TSOP leads
14 and the contacting exposed conductors of the bonded flexible circuit.

15 Each layer is completed before stacking. Ordinarily, pre-tested
16 TSOP's can be used, eliminating the requirement for testing. For special
17 applications, additional testing may conveniently be accomplished by testing the
18 ball grid array layer using a production-testing fixture which contacts the ball
19 grid contacts. Functional testing may include:

20 Testing at extreme temperatures (e.g., minus 55°C to plus 125°C);

21 Burned in (both temperature and bias); and

22 Environmentally screened (i.e., temperature cycle, thermal shock,
23 humidity, bias)

1 The availability of the full top and bottom surfaces of the layer for
2 ball grid terminals, the ability to transpose connections to different ball grid
3 contact positions by arranging the geometry of the conductors in the flexible
4 circuit, and the large number of vertical interconnections, allow for a very high
5 input/output (I/O) count to accommodate the needs of the stacked IC's.

6 Further, this application discloses stacked IC-containing devices
7 having a smaller footprint than the original TSOP's used to make them, and
8 methods for stacking the IC-containing layers to produce stacked IC-containing
9 devices.

10

11 Brief Description of the Drawings

12 Figure 1 shows a side view of a standard TSOP and a TSOP with
13 the leads trimmed.

14 Figure 2 shows a side view of the TSOP after rounding of the
15 package edges.

16 Figure 3 shows a partial view of a flexible polyamide/metal
17 conductor circuit.

18 Figure 4 shows an exploded view of a severed conductor in the
19 polyamide hole.

20 Figure 5 shows a side view of flexible circuit of figure 3 before hot
21 forming, and the same circuit after hot forming around the TSOP.

22 Figure 6 shows a top view and side view of the BGA/TSOP
23 assembly complete with two flexible circuits formed and bonded to it.

1 Figure 7 shows an example four-high stack of BGAT SOP
2 assemblies with their BGA contacts joined with solder connections.

3 Figure 8 shows two layers of a flexible circuit and illustrates the
4 ability to make unique contact to upper layers in a stack.

5

6

7 Detailed Description

8 This invention consists of a stack of semiconductor IC's electrically
9 and mechanically interconnected in the vertical direction. The end user of this
10 stack will connect it to a substrate such as a printed circuit board (PCB). The
11 vertical placement of IC's will save considerable substrate area as opposed to
12 the conventional horizontal placement of an equivalent number of IC's on the
13 substrate.

14 Each layer within the stack will consist of an off-the-shelf
15 commercially available IC 1 in a thin small outline package (TSOP) processed
16 in such a manner as to route the TSOP's electrical input/output (I/O)
17 connections from the leads on the sides or the ends of the package to an array
18 of metallic bumps or a ball grid array (BGA) on both the top surface and the
19 bottom surface of the TSOP package. The routing process consists of the
20 following steps:

21 Trim the TSOP's leads close to the TSOP body to approximately
22 .015". A trimmed TSOP 2 is illustrated in Figure 1.

23 The edges of the TSOP package may be optionally rounded 3 to

1 reduce the bending radius of the polyimide/conductor circuit to be applied in
2 step 7. A rounded TSOP package 3 is illustrated in Figure 2. Fabricate a
3 polyimide/metal conductor circuit 4 as shown in figure 3 containing conductors
4 with ends that, through vias in the polyimide, terminate on metal balls or bumps
5 5 (achieved by electroplating or other methods). There is a hole in the polyimide
6 6 exposing a conductor element 7 near their mid-section where the conductor is
7 intended to be joined with the TSOP leads on one side or end of the package. A
8 second circuit will be fabricated to contact the leads on the opposite side or end
9 of the TSOP package.

10 Using an appropriate fixture, sever the conductors 7 exposed in
11 holes in the polyimide as shown in Figure 4.

12 Using an appropriate heated fixture resembling the approximate
13 shape of the TSOP, hot form the polyimide/metal conductor circuit into such a
14 shape that it will slip over one of the lead edges of the TSOP 8 as shown in
15 Figure 5. A second polyimide/conductor circuit similarly formed 9 will slip over
16 the second lead edge of the TSOP.

17 Apply a thermosetting epoxy adhesive to the top and bottom sides
18 of the TSOP and partially cure the adhesive.

19 Slide the hot formed polyimide/metal conductor circuits over each
20 side of the TSOP such that the trimmed TSOP leads penetrate the polyimide
21 holes in the circuit and contact the severed metal conductors 10.

22 Using an appropriate fixture to hold the assembly in place, cure
23 the epoxy adhesive 11 as shown in Figure 6.

1 Dip the edges of the TSOP having leads into a high melting
2 temperature solder 12 to accomplish an electrical connection between the
3 TSOP trimmed leads and the severed and formed metal conductors within the
4 polyimide/metal conductor circuit as shown in Figure 6.

5 At this point the TSOP's electrical connections have been re-
6 routed from the leads on the sides or ends of the body to a BGA on the top
7 surface and/or the bottom surface of the TSOP's. It should be noted that not all
8 bumps or balls 5 in the BGA are to be connected to a TSOP lead. Some
9 conductors will use the space between leads simply to connect a ball or bump
10 on the top TSOP surface with a ball or bump on the bottom TSOP surface.
11 When the TSOP's are stacked, this allows for independent electrical connection
12 from the bottom of the stack to individual TSOP's in the stack.

13 The processed TSOP's are now ready for stacking which is
14 accomplished by printing or dispensing a high melting point solder part to the
15 BGA locations on the top surface and/or the bottom surface of the processed
16 TSOP's and then reflowing the solder paste in a convection or vapor phase
17 reflow furnace (see figure 7). The solder 14 used in stacking and in connecting
18 the polyimide/conductor circuit to the TSOP leads should have a melting point
19 higher than the temperature the end user will use to connect the stack to the
20 substrate.

21 What is unique about this invention is that it stacks TSOP's in a
22 footprint smaller than the TSOP footprint itself and that the BGA interconnection
23 between the layers of the stack provides for a large number of non-common

1 (non-bussed) connections between individual layers themselves and individual
2 layers and the substrate to which the stack is attached.

3 Figure 8 demonstrates how electrical contact 14 can be made
4 vertically in the stack so as to connect each TSOP's pin 1 in common and bring
5 it to the base of the stack. It also demonstrates how the pin 2 of a layer 1 TSOP
6 15 and pin 2 of a layer 2 TSOP 16 can each be brought out separately to
7 different locations at the base of the stack. This re-route scheme continues for
8 multiple layers of the stack enabling the ability to expand memory depth and
9 memory width beyond that of the TSOP's in the stack and to stack IC's (other
10 than memory) in the stack.

11 From the foregoing description, it will be apparent that the device
12 and method disclosed in this application will provide the significant functional
13 benefits summarized in the introductory portion of the specification.

14 The following claims are intended not only to cover the specific
15 embodiments disclosed, but also to cover the inventive concepts explained
16 herein with the maximum breadth and comprehensiveness permitted by the
17 prior art.

18

1 4. The structure of claim 1 in which:
2 flat bump connectors are used instead of ball grid connectors.

1 5. The structure of claim 1, in which:
2 one or more terminal-bearing sides of the TSOP in one or more
3 layers are mechanically rounded to increase the bending
4 radius of the flexible circuit.

1 6. A method of manufacturing an IC-containing layer ready for
2 stacking with other layers in order to provide a dense electronic package,
3 comprising the steps of:
4 fabricating a flexible circuit with its electrical conductors disposed
5 to provide the desired connector geometry for connection of
6 a TSOP with other layers;
7 forming the flexible circuit so that it fits over a lead-bearing side of
8 a TSOP; and
9 bonding the flexible circuit to the TSOP so as to align exposed
10 conductors of the flexible circuit in solderable contact with
11 the TSOP leads.

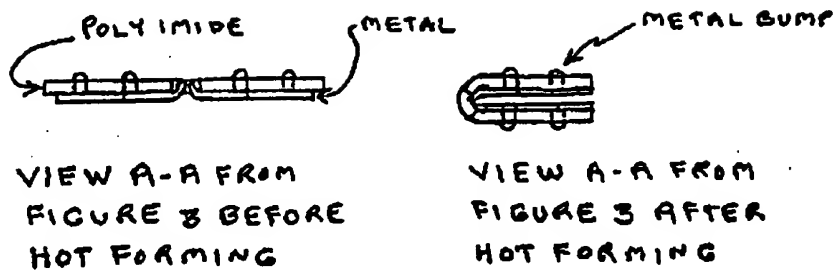
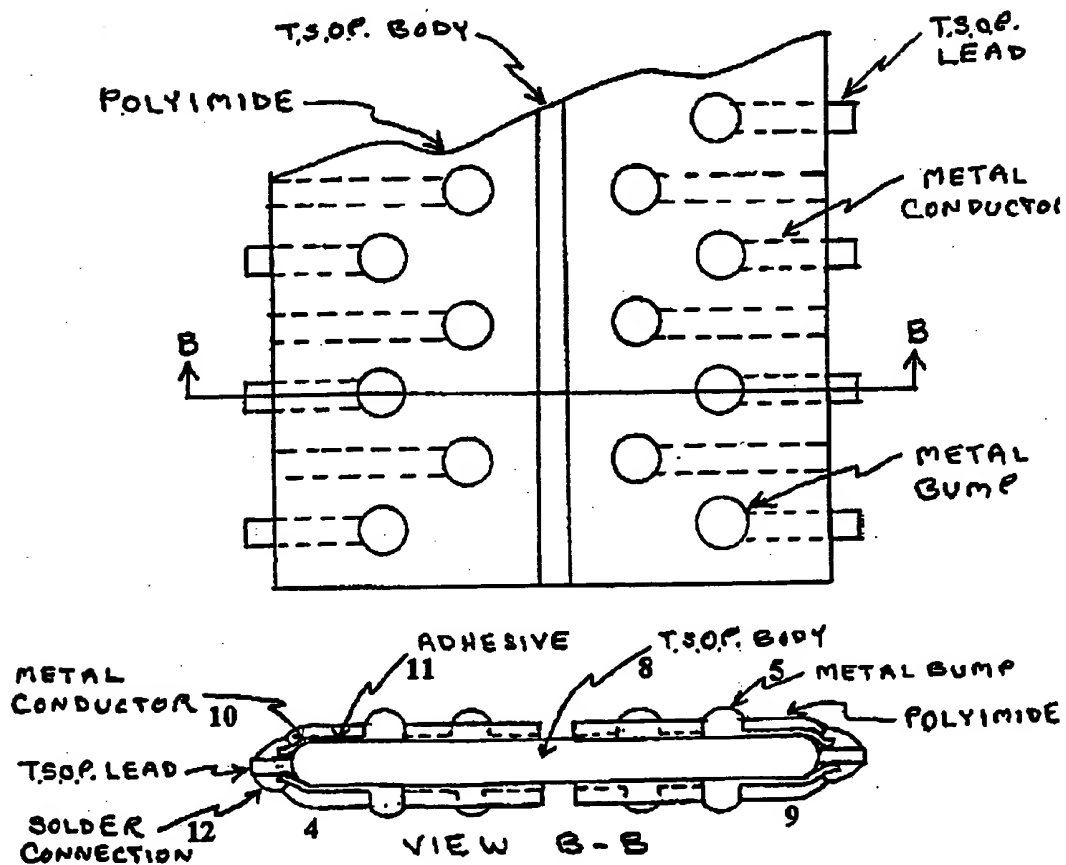
1 7. The method of claim 6 which also comprises:
2 fabricating, forming, and bonding a second flexible circuit over the
3 other lead-bearing side of a TSOP

What is claimed is:

1 1. A stack of IC chip-enclosing layers, comprising:
2 an IC-containing layer comprising:
3 a TSOP containing one or more IC chips and having I/O terminals
4 thereon; and
5 a flexible circuit, with exposed solderable contacts for connection
6 to the TSOP terminals and ball grid contacts for connection
7 with other layers in the stack, formed to fit over each
8 terminal-bearing side of the TSOP; and
9 a second IC-containing layer with ball grid contacts, supported on
10 top of the lower layer and connected to the first layer via
11 their respective ball grid contacts.

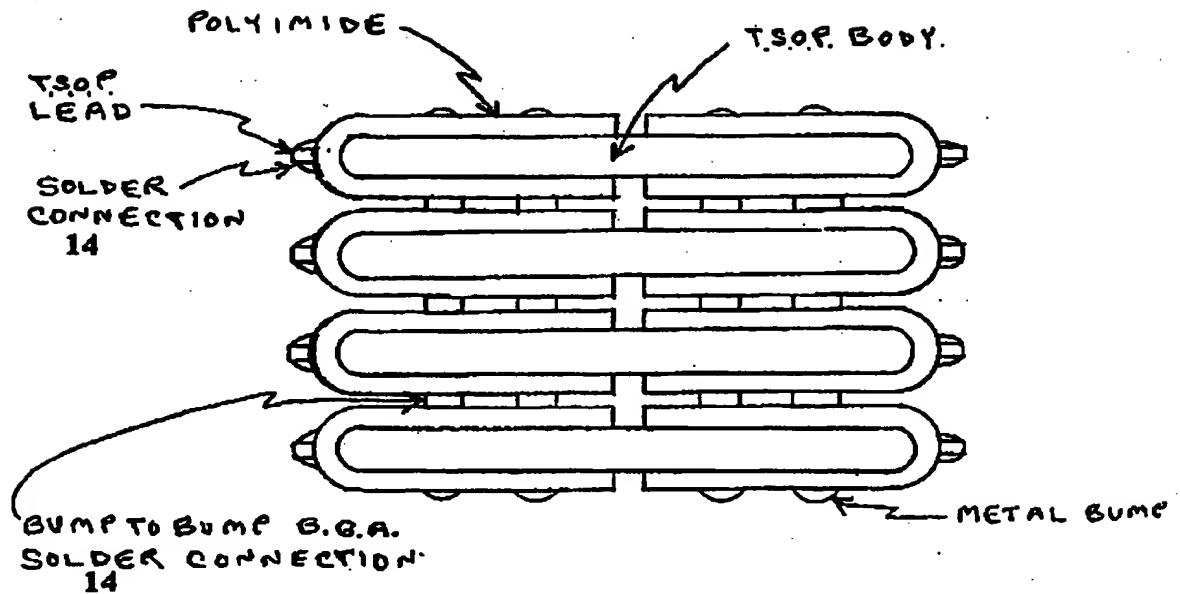
1 2. The structure of claim 1 in which:
2 additional IC chip-containing layers are supported and connected
3 on the top of the second layer.

1 3. The structure of claim 1 in which:
2 the ball grid contacts on the upper surface of one or more layers
3 do not all electrically connect with the corresponding ball
4 grid contacts on the lower surface of the layer.

FIGURE 5

POLYIMIDE/METAL CIRCUITS
ATTACHED TO T.S.O.P.

FIGURE 6



FOUR HIGH STACK OF T.S.O.P.
ASSEMBLIES WITH B.G.A.'S
SOLDER CONNECTED

FIGURE 7

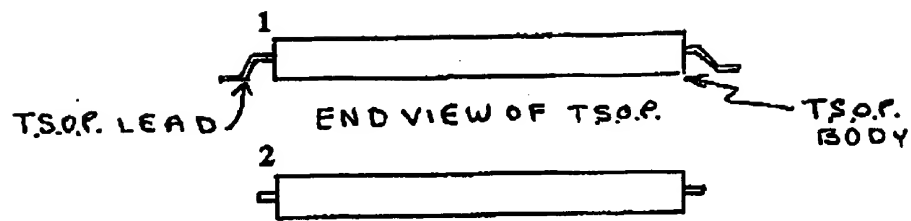


FIGURE 1

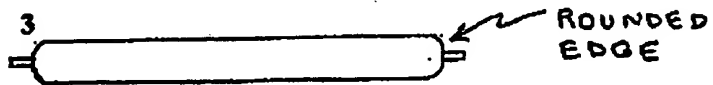


FIGURE 2

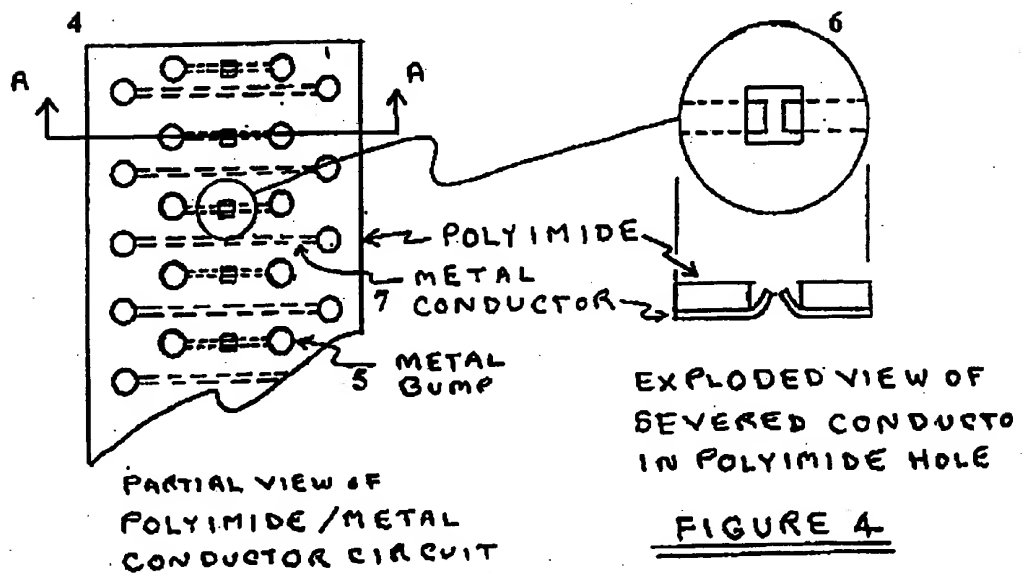


FIGURE 3

1 8. The method of claim 7 in which the flexible circuits provide a
2 ball grid array covering the entire top and bottom of the layer.

1 9. The method of claim 6 which also comprises:
2 stacking a plurality of the layers; and
3 electrically interconnecting conductors in each layer with
4 conductors in the adjacent layer.

1 10. The method of claim 9 in which pre-tested TSOP's are
2 utilized.

1 11. The method of claim 9 which also comprises:
2 testing, prior to stacking, for performance of the circuitry of each
3 layer to establish the layer as a known good element.

1 12. The method of claim 11 in which the performance testing
2 includes testing at extreme temperatures, testing through thermal cycles and
3 thermal shock, and testing for performance under humidity conditions.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US99/13171

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H05K 1/11; H01L 23/12

US CL :257/686, 777; 361/749, 803; 439/67

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/686, 777; 361/749, 776, 803; 439/67, 77

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A,P	US 5,835,359 A (DiFRANCESCO) 10 NOVEMBER 1998 (10.11.98), Fig. 7D, col.13, line 18-col.14, line 3.	1,6
A,P	US 5,776,797 A (NICEWARNER, JR. et al.) 07 JULY 1998 (07.07.98), Fig. 7.	1,6
A	US 5,598,033 A (BEHLEN et al.) 28 JANUARY 1997 (28.01.97), Fig. 4.	1-12
A	US 5,394,303 A (YAMAJI) 28 FEBRUARY 1995 (28.02.95), Fig. 8.	1,6
A	US 3,492,538 A (FERGUSON) 27 JANUARY 1970 (27.01.70), Figs. 1 and 2.	1,6
A	US 3,221,286 A (FEDDE) 30 NOVEMBER 1965 (30.11.65), Figs. 2 and 3.	1,6



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:	T	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
A document defining the general state of the art which is not considered to be of particular relevance	X	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
E earlier document published on or after the international filing date	Y	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	A*	document member of the same patent family
O document referring to an oral disclosure, use, exhibition or other means		
P document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search

13 OCTOBER 1999

Date of mailing of the international search report

03 NOV 1999

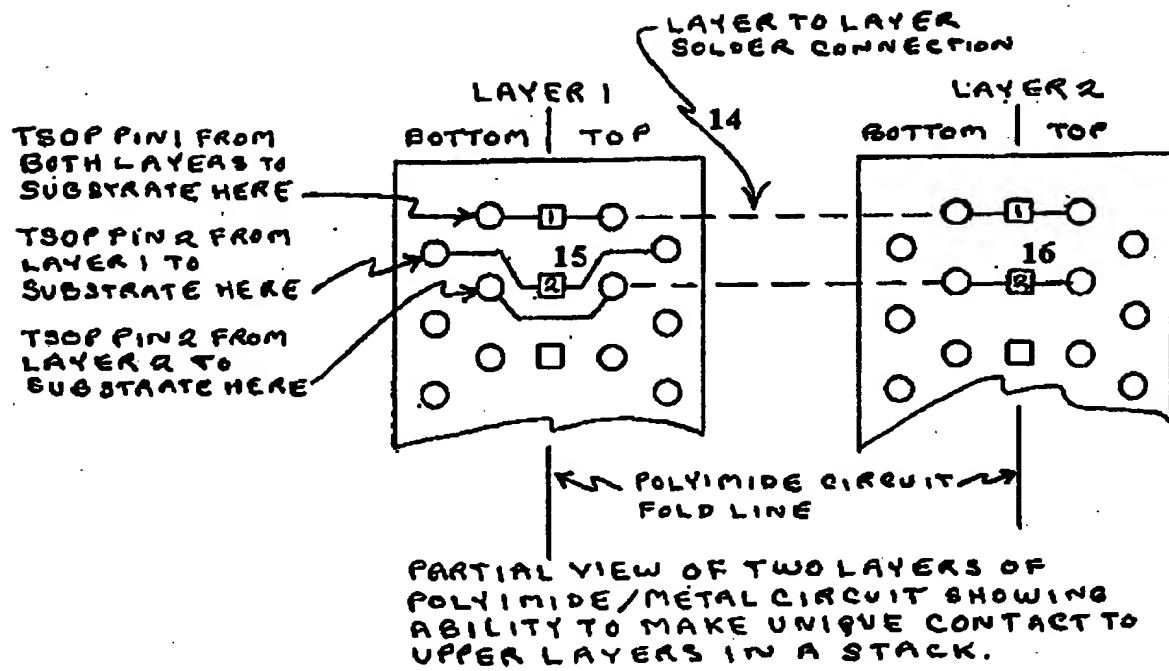
Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

Facsimile No. (703) 305-3230

Authorized officer

JOHN B. VIGUSHIN

Telephone No. (703) 308-1782

FIGURE 8

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ **BLACK BORDERS**
- ☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- ☐ **FADED TEXT OR DRAWING**
- ☐ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- ☐ **SKEWED/SLANTED IMAGES**
- ☐ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- ☐ **GRAY SCALE DOCUMENTS**
- ☐ **LINES OR MARKS ON ORIGINAL DOCUMENT**
- ☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- ☐ **OTHER:** _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.

This Page Blank (uspto)